Smalltalk Debug Lives in the Matrix

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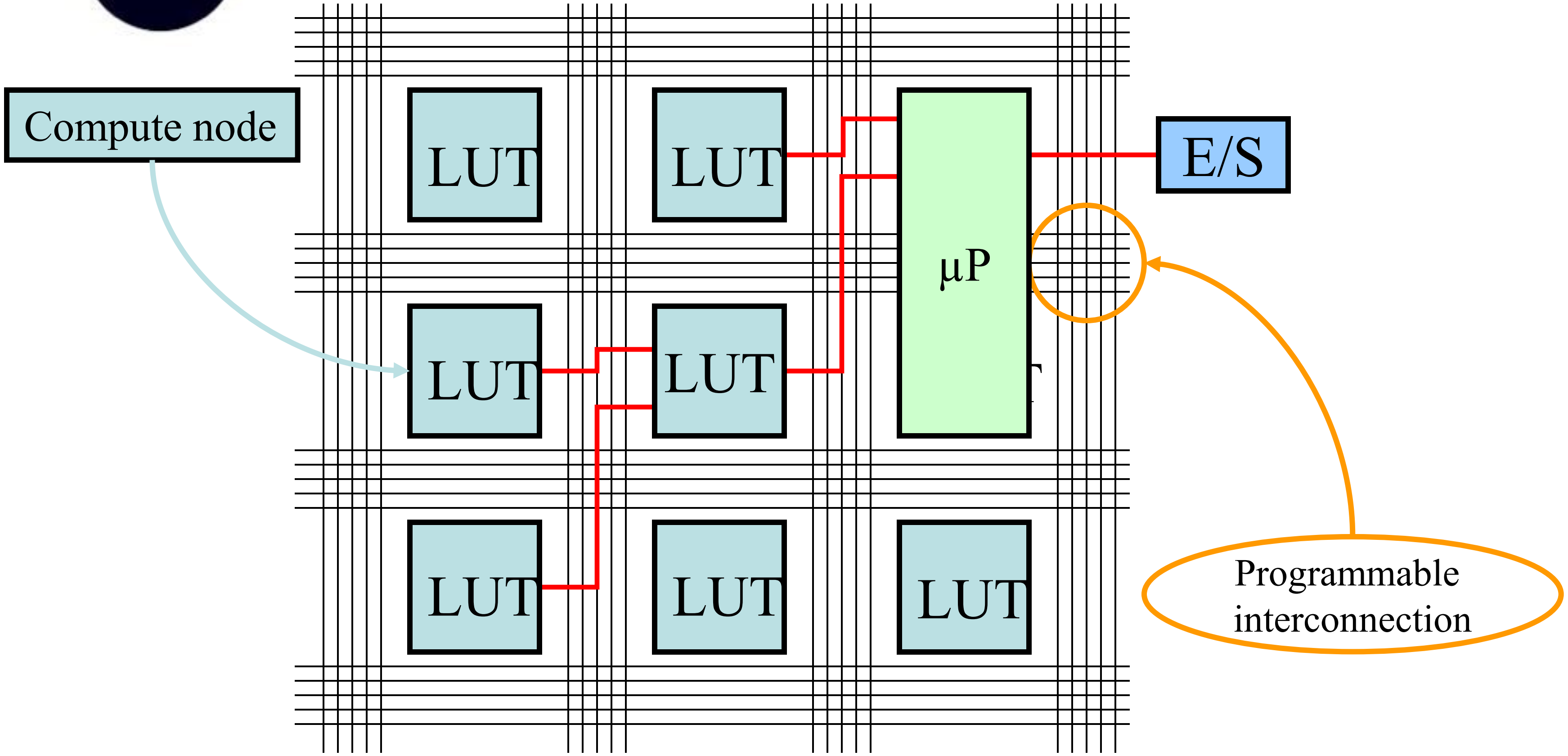
What Matrix?

+ "Flexible" hardware
  Time to market

− Hard to program
  Hard to debug



What Matrix?

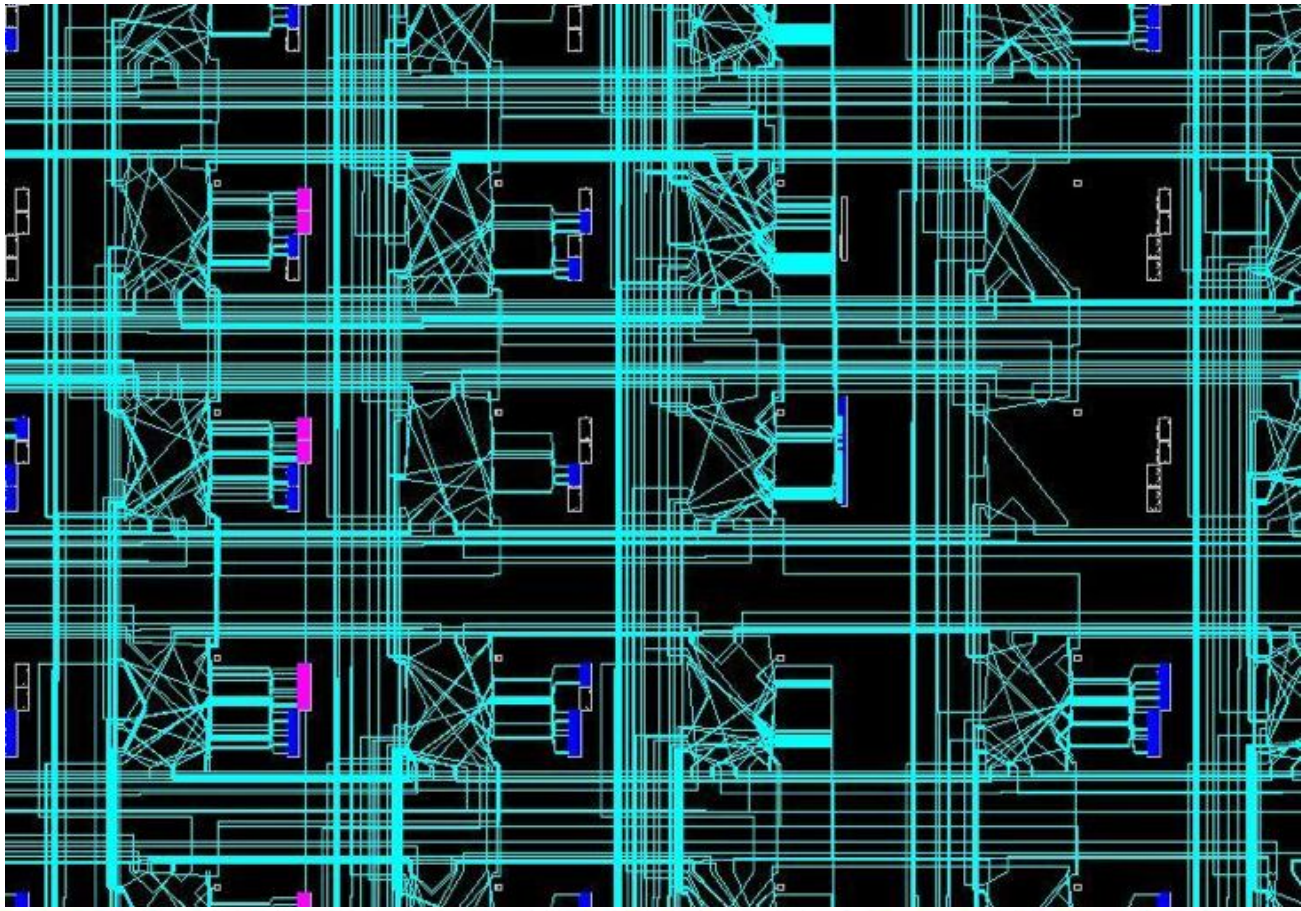
➕ "Flexible" hardware
Time to market

➖ Hard to program
Hard to debug

Specific languages
Specific tools

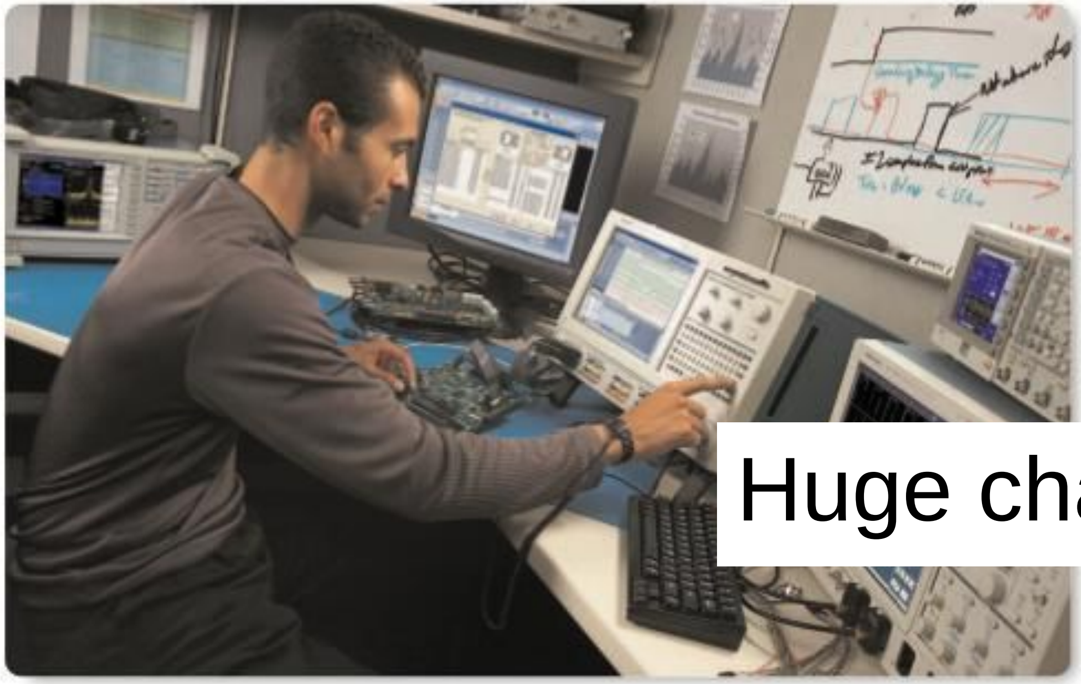
Performances still requires manual tuning

EE skills required



State of the art debugging

Simplifying Xilinx and Altera FPGA Debug

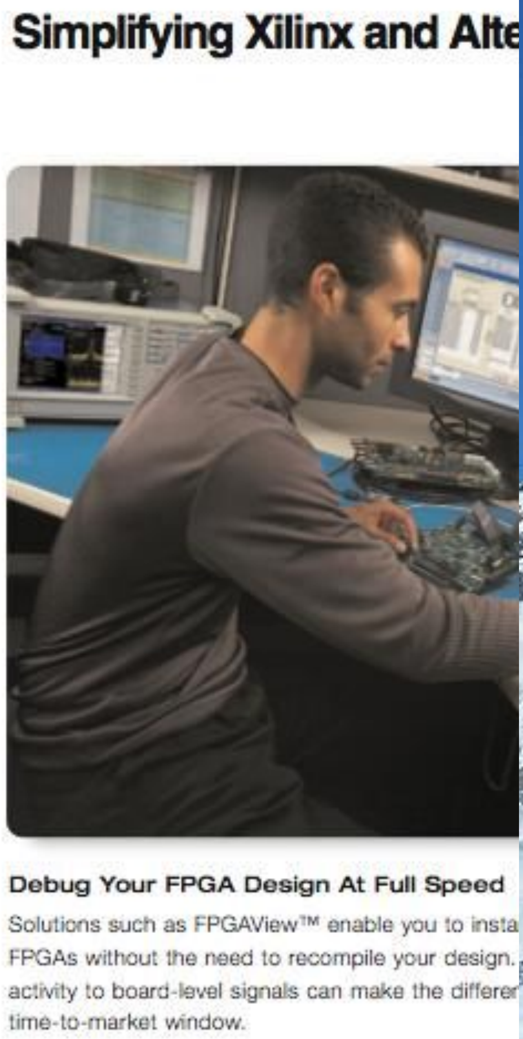


Huge challenge

Debug Your FPGA Design At Full Speed

Solutions such as FPGAView™ enable you to instantly move probe points within your Xilinx and Altera FPGAs without the need to recompile your design. Plus the ability to correlate internal FPGA signal activity to board-level signals can make the difference between hitting your schedule and missing your time-to-market window.

Touching the void


Simplifying Xilinx and Alte

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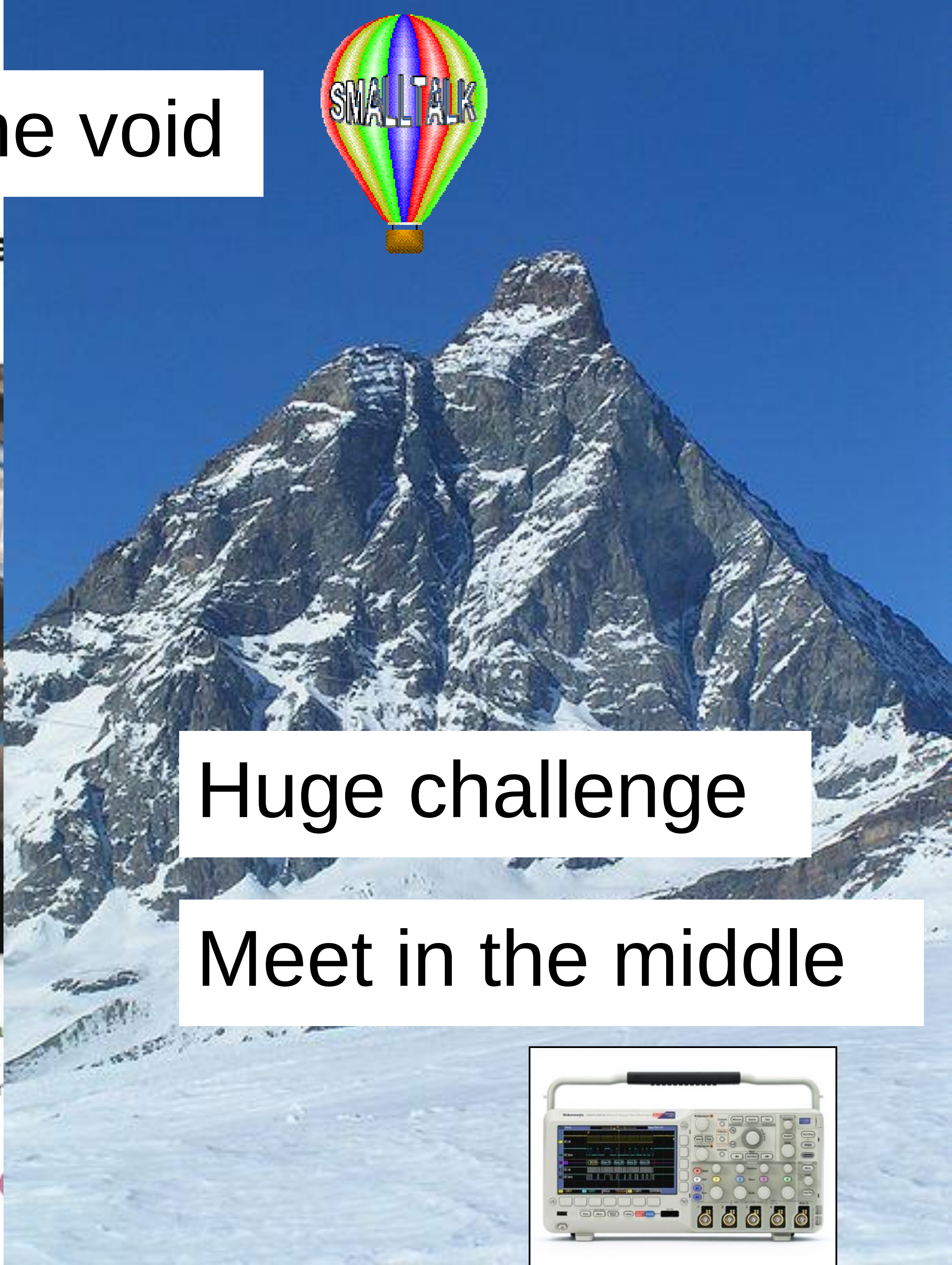


Huge challenge

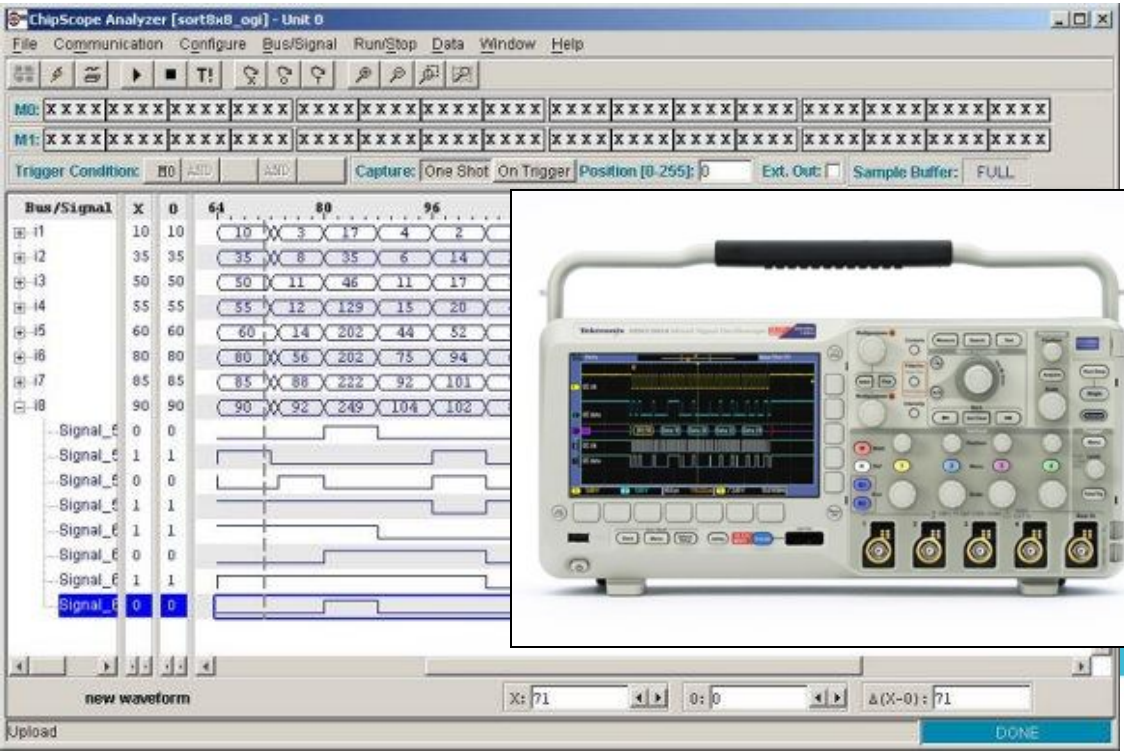
Meet in the middle

Debug silver bullet

- Observability
- Controlability
- Abstract analysis
- Fast changes

Extreme Programming

```
Debugging
1 run, 0 passed, 0 failed, 1 error
BowlingTest>>#testAllGutters
```


ChipScope Analyzer [sort8x8_ogi] - Unit 0
File Communication Configure Bus/Signal Run/Stop Data Window Help
Trigger Condition:
Capture: One Shot On Trigger Position [0-255]: 0
Ext. Out:
Sample Buffer: FULL
Bus/Signal
new waveform
Upload
DONE

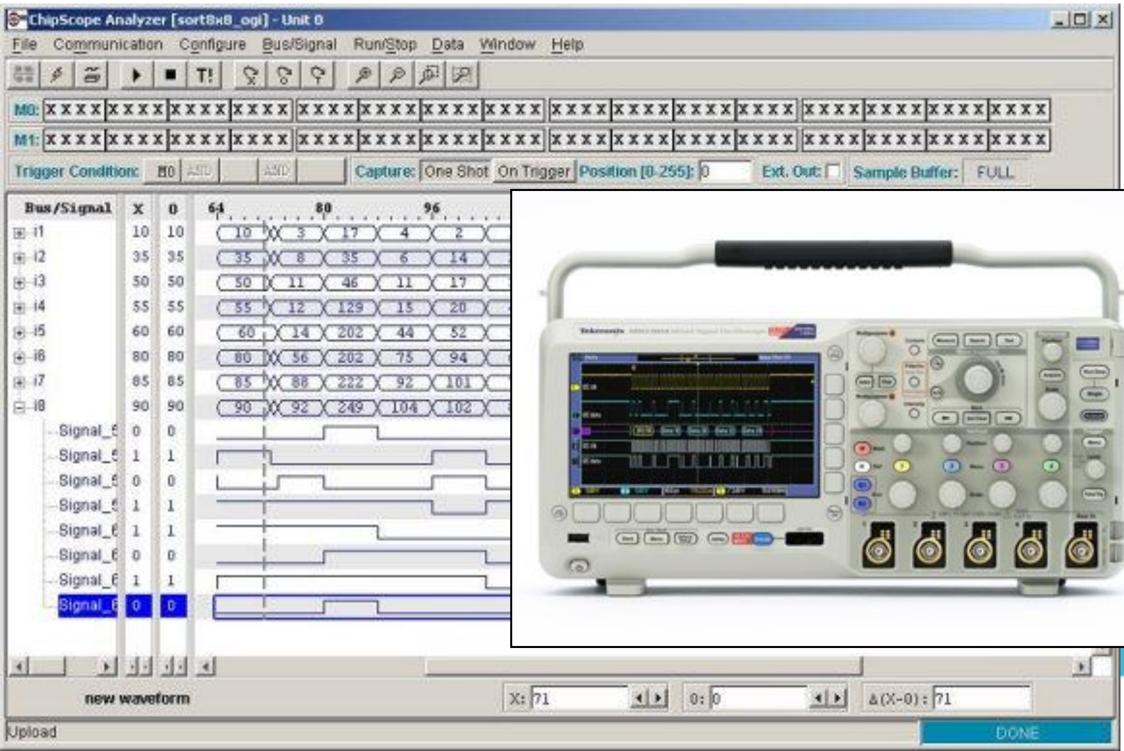
- Time to market
- Multiple runs
- Long cycles
- Simulation is not enough

Debug silver bullet

- Observability
- Controlability
- Abstract analysis
- Fast changes

Extreme Programming

SUnit Camp Smalltalk 3.1 TestRunner
Refresh
BowlingTest
Run
RunAll
Debugging
1 run, 0 passed, 0 failed, 1 error
BowlingTest>>#testAllGutters
Debug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File Communication Configure Bus/Signal Run/Stop Data Window Help
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Ext. Out:
Sample Buffer: FULL
Bus/Signal
new waveform
X: 71
0: 0
Δ(X-0): 71
Upload
DONE

- Time to mar
- Multiple r
- Long
- Si is not

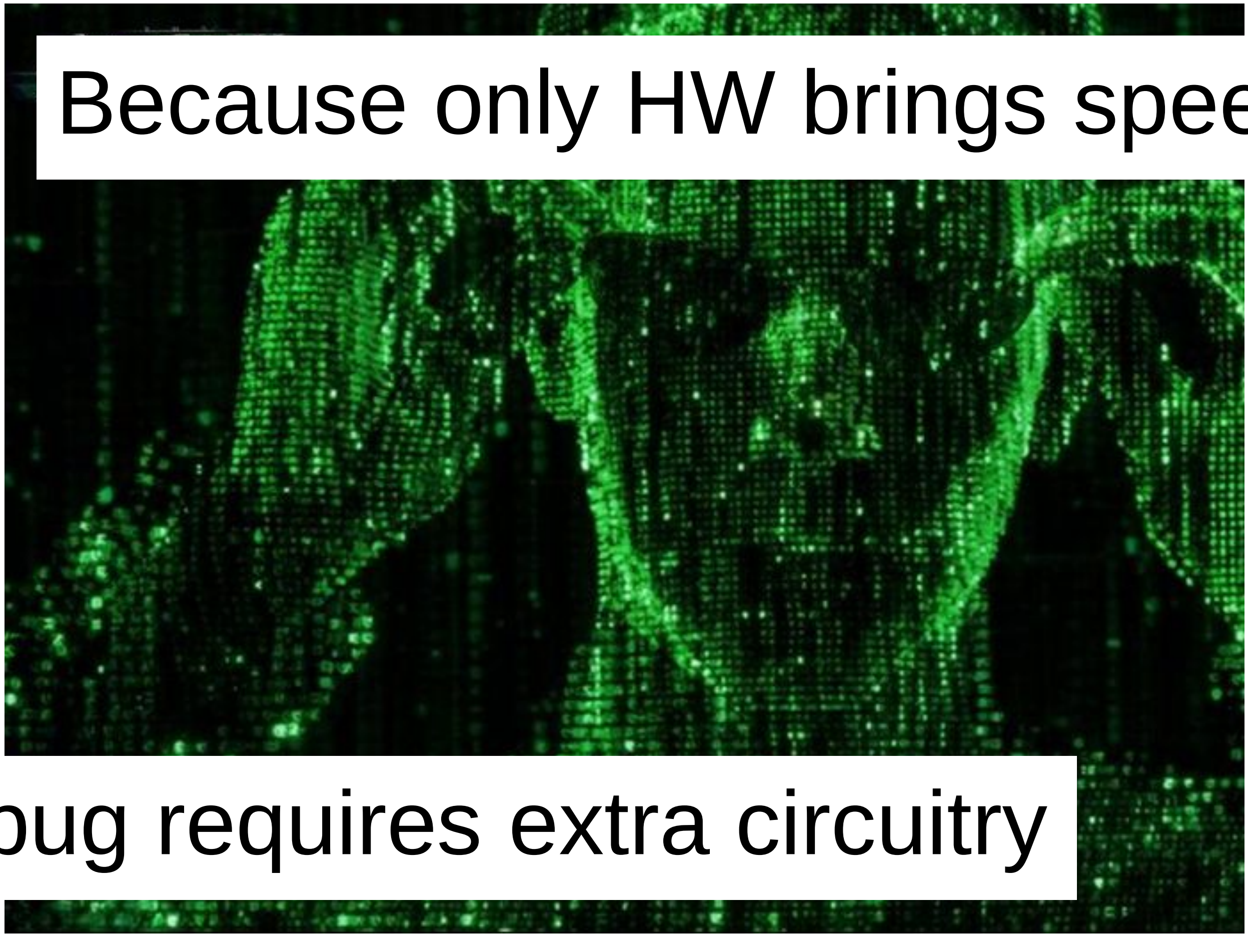
New challenges :
Threat or opportunity?

Operate at-speed

Keep your speed-up alive

Multiple runs prohibit any over time penalty

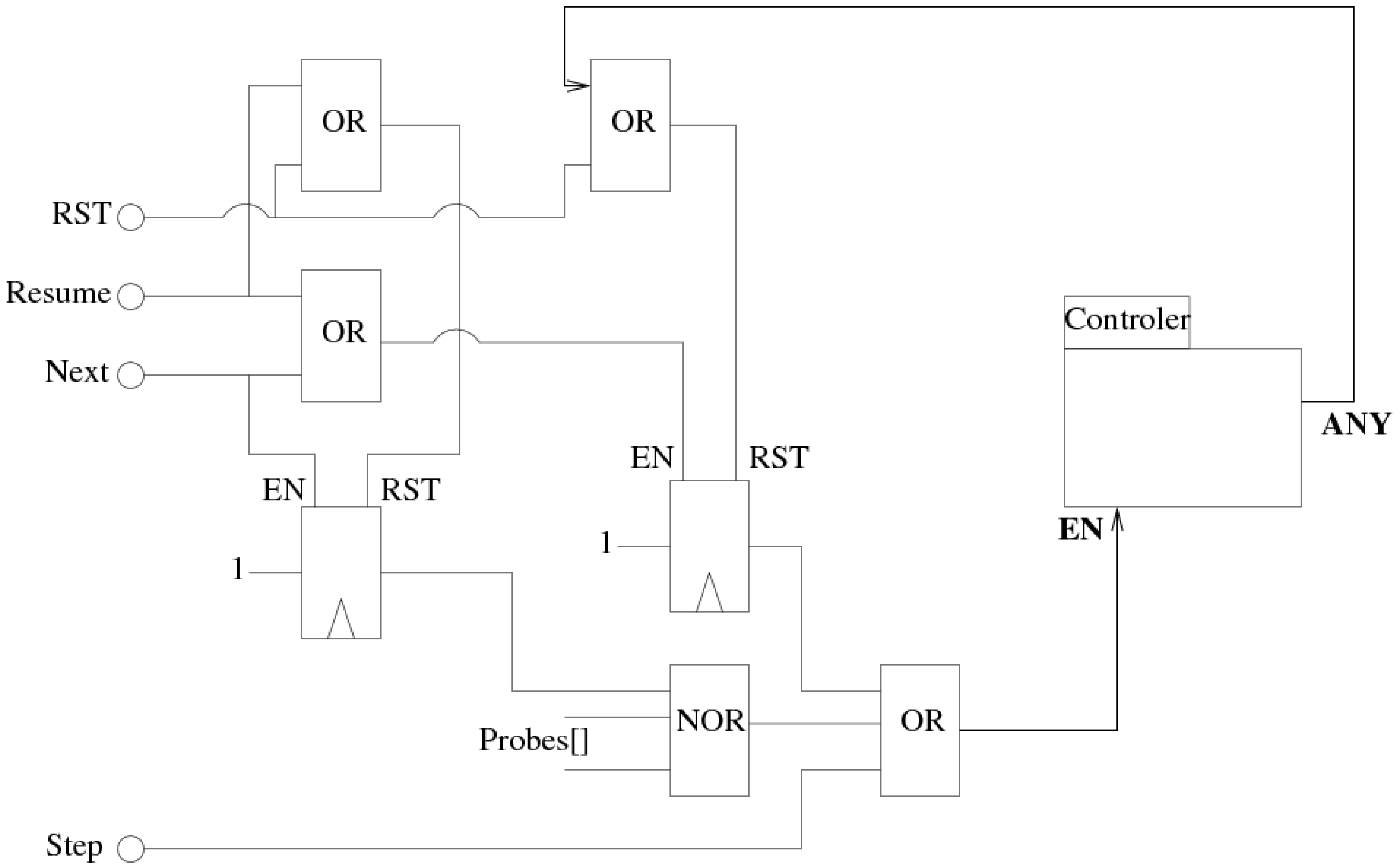
Operate in-situ



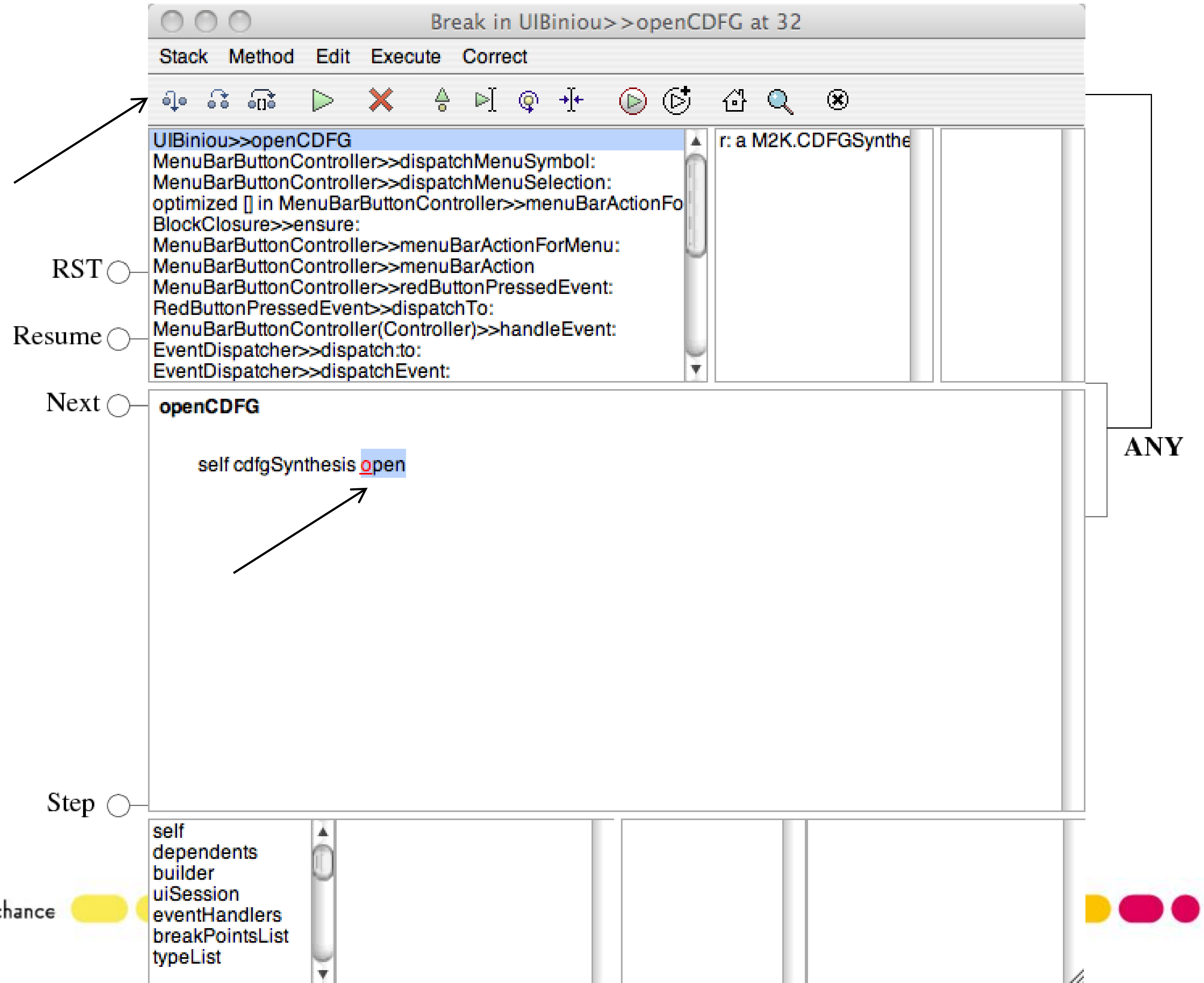
Because only HW brings speed-up

Debug requires extra circuitry

Debugging facilities are circuits



Debugging facilities are circuits



Break in UIBiniou>>openCDFG at 32

```
UIBiniou>>openCDFG
MenuBarButtonController>>dispatchMenuSymbol:
MenuBarButtonController>>dispatchMenuSelection:
optimized [] in MenuBarButtonController>>menuBarActionFo
BlockClosure>>ensure:
MenuBarButtonController>>menuBarActionForMenu:
MenuBarButtonController>>menuBarAction
MenuBarButtonController>>redButtonPressedEvent:
RedButtonPressedEvent>>dispatchTo:
MenuBarButtonController(Controller)>>handleEvent:
EventDispatcher>>dispatch:to:
EventDispatcher>>dispatchEvent:
```

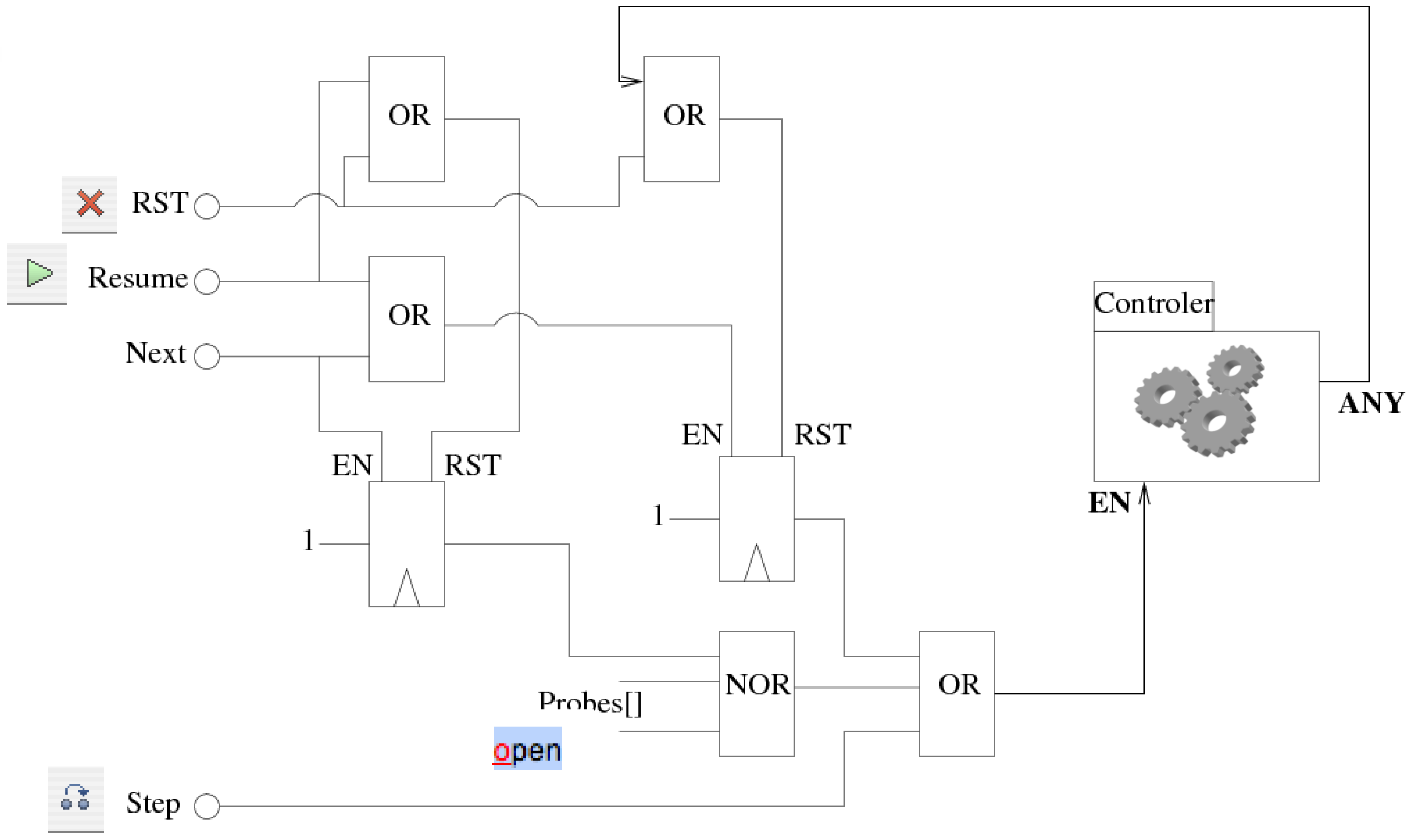
r: a M2K.CDFGSynthe

```
openCDFG

    self cdfgSynthesis open
```

```
self
dependents
builder
uiSession
eventHandlers
breakPointsList
typeList
```

Debugging facilities are circuits

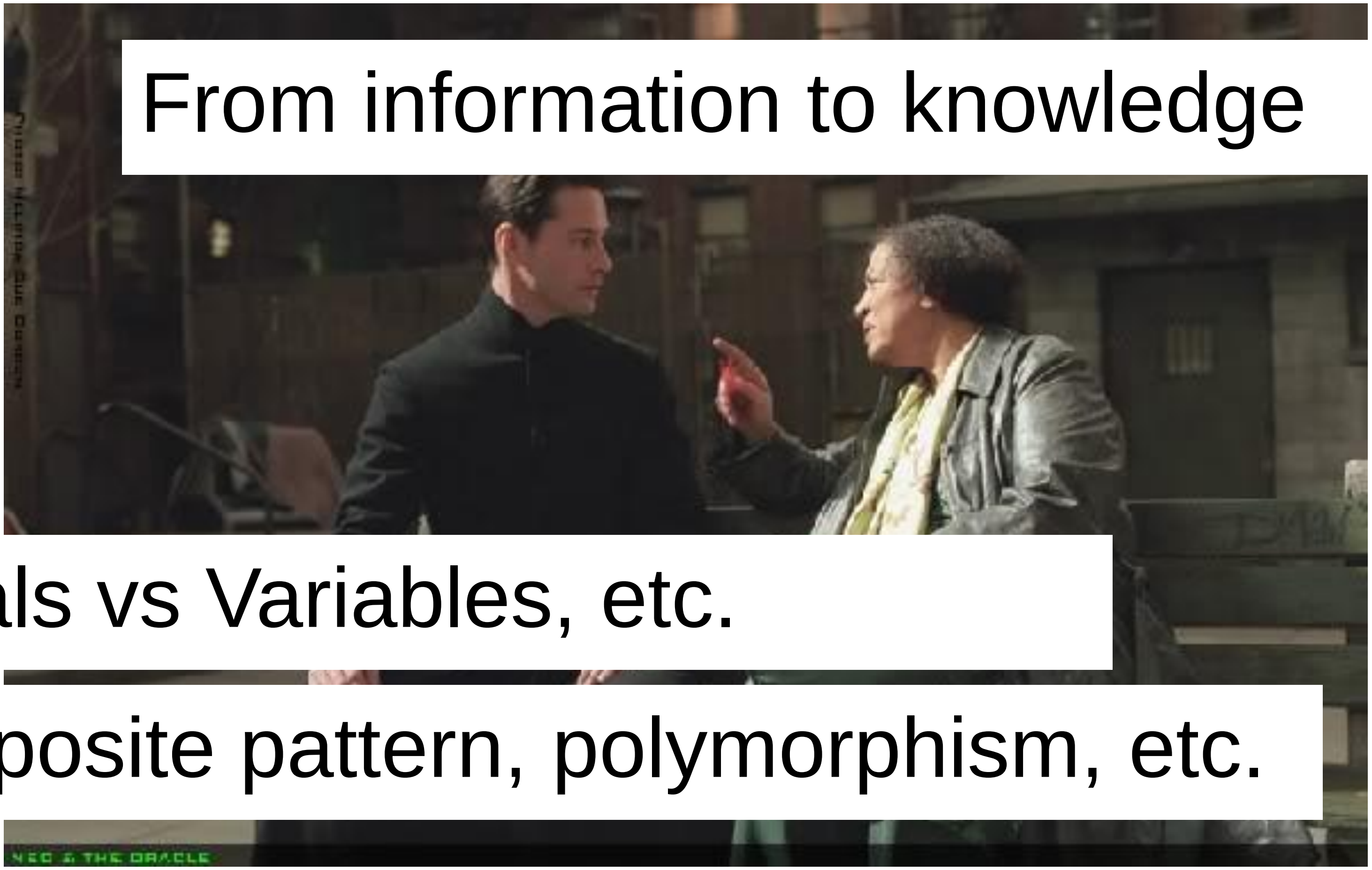


Observe and monitor

Take decision

You cannot watch everything

Abstract analysis: semantic needed

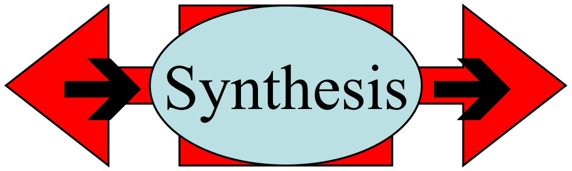


From information to knowledge

Signals vs Variables, etc.

Composite pattern, polymorphism, etc.

From a technical point of view



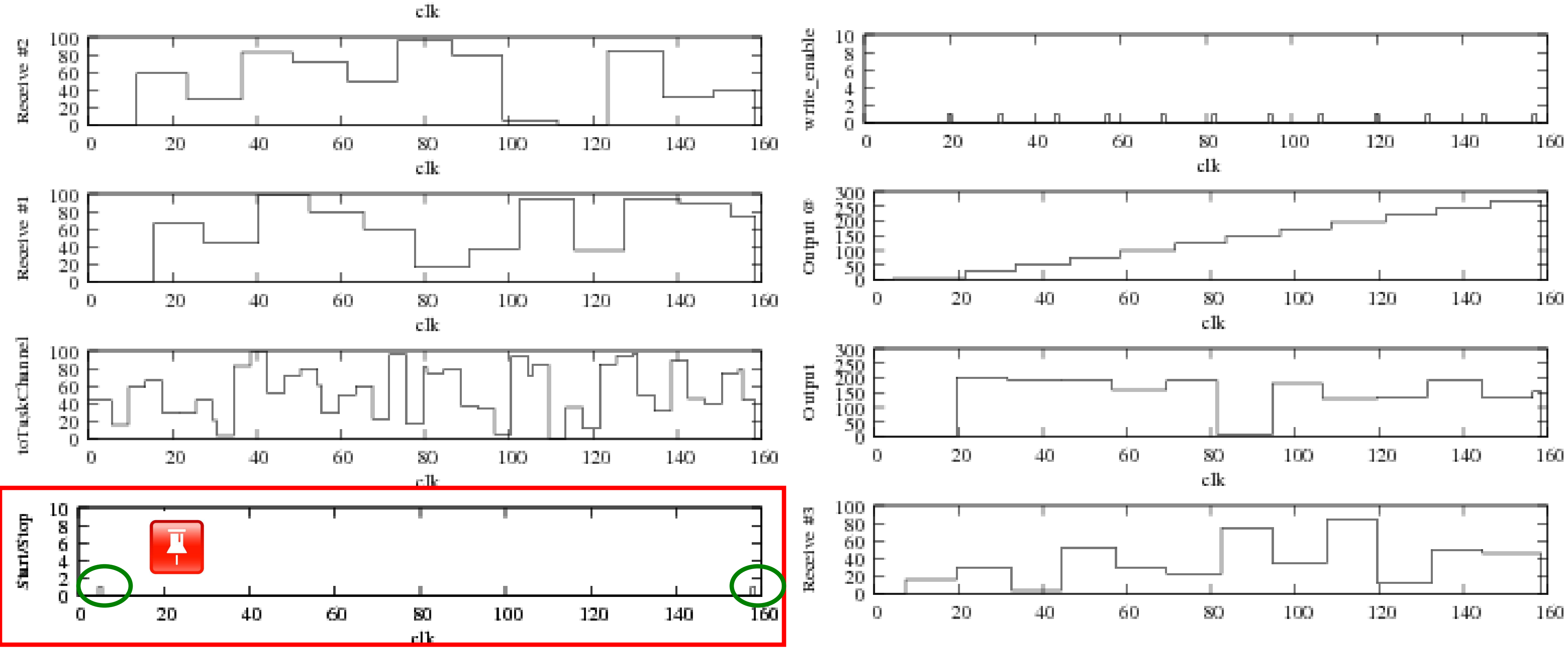
Software abstraction

Implementation in hardware

From D. Picard's ESUG 2009 talk

Full observabiliy isn’t scalable

Focus on POI



Full observabiliy isn't scalable

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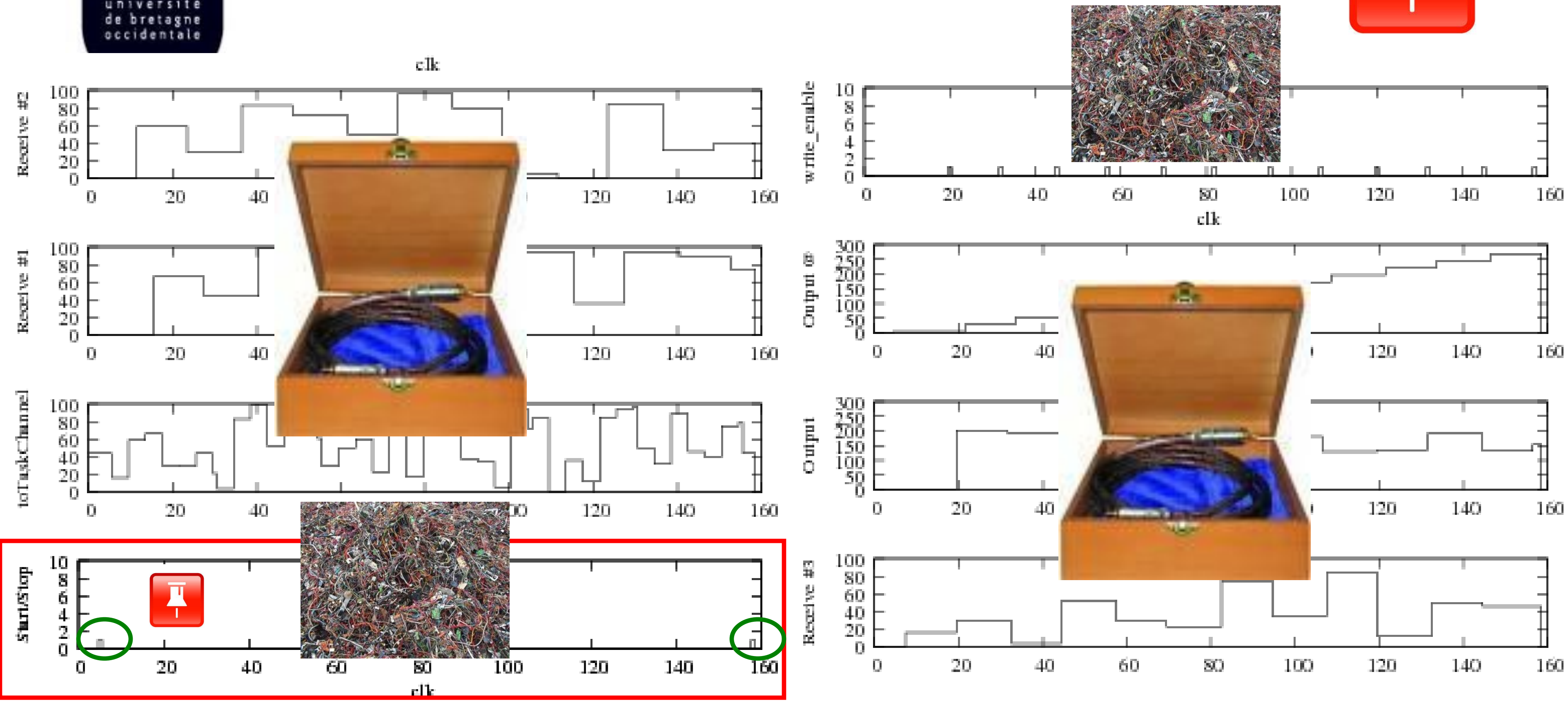
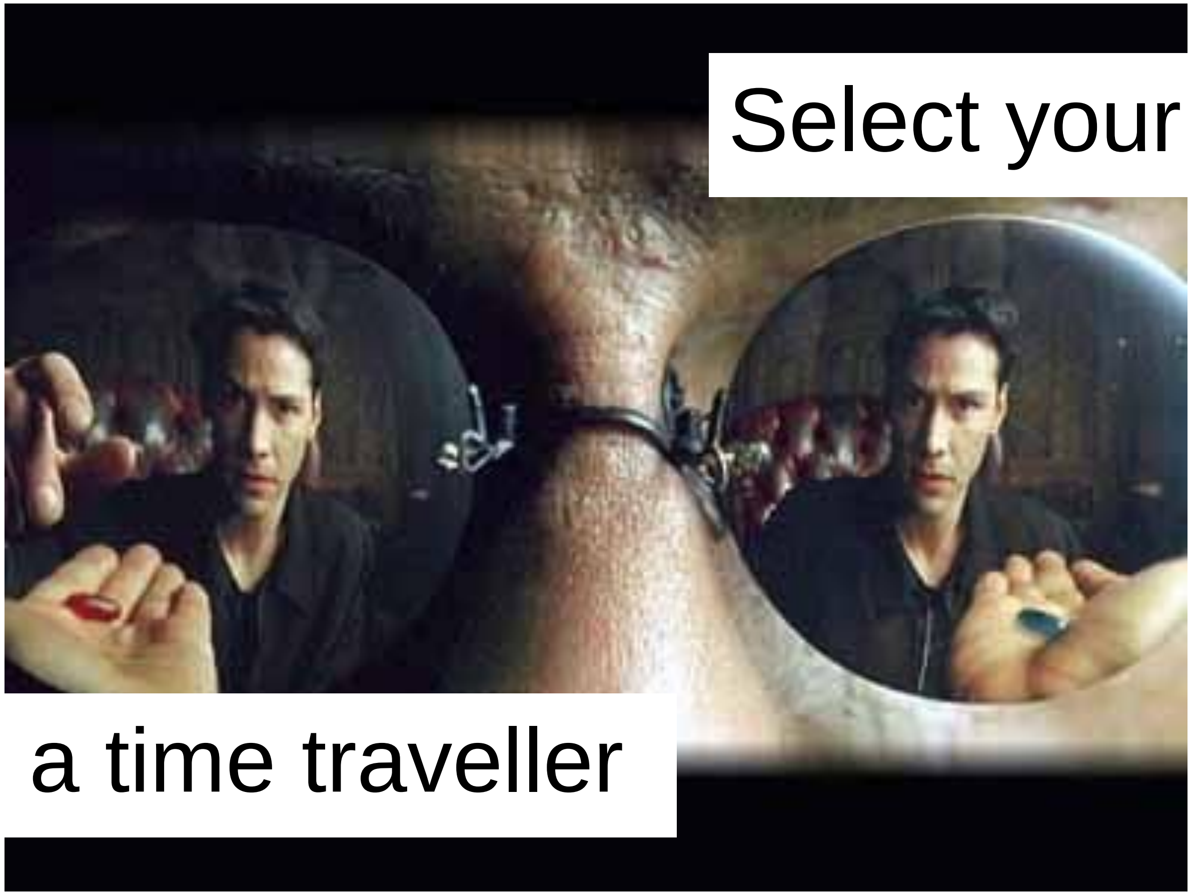


Take control



Select your

Become a time traveller

Smalltalk debugger

- Just fit approach
- Run code and catch exception
- Code hot replacement, variable update, etc.
- Step on or resume execution
- Possible rollback

- Multiple runs
- Breakpoints update, earlier exception
- Same conceptual behavior

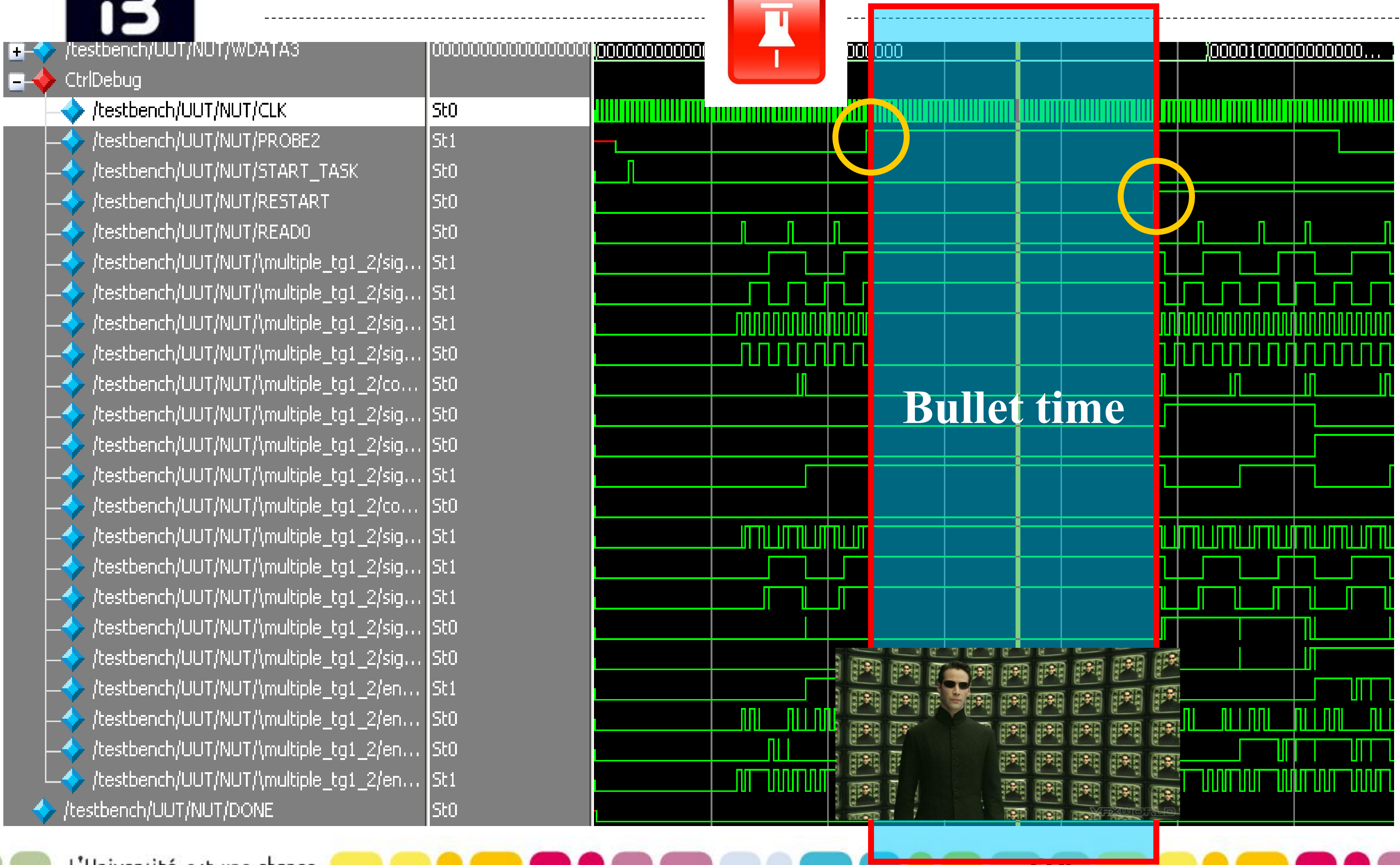
Become a time traveller

Dodge bullets

Once the time has stopped

… just operate !

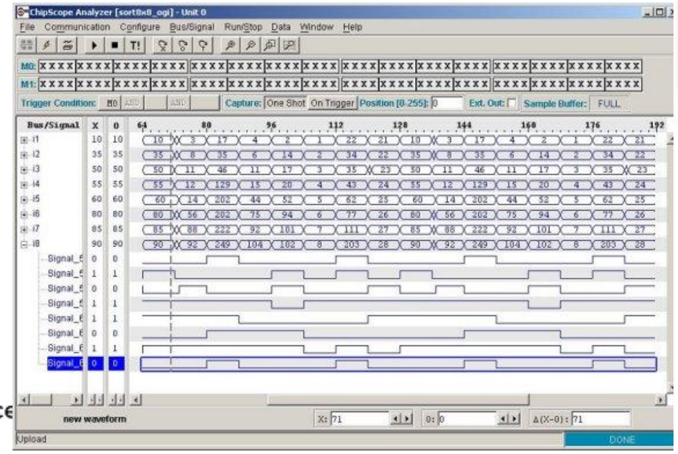
Bullet time explained



```
+ /testbench/UUT/NUT/WDATA3                         0000000000000000
- CtrlDebug
    /testbench/UUT/NUT/CLK                          St0
    /testbench/UUT/NUT/PROBE2                       St1
    /testbench/UUT/NUT/START_TASK                   St0
    /testbench/UUT/NUT/RESTART                      St0
    /testbench/UUT/NUT/READ0                        St0
    /testbench/UUT/NUT/\multiple_tg1_2/sig...       St1
    /testbench/UUT/NUT/\multiple_tg1_2/sig...       St1
    /testbench/UUT/NUT/\multiple_tg1_2/sig...       St1
    /testbench/UUT/NUT/\multiple_tg1_2/sig...       St0
    /testbench/UUT/NUT/\multiple_tg1_2/co...        St0
    /testbench/UUT/NUT/\multiple_tg1_2/sig...       St0
    /testbench/UUT/NUT/\multiple_tg1_2/sig...       St0
    /testbench/UUT/NUT/\multiple_tg1_2/sig...       St1
    /testbench/UUT/NUT/\multiple_tg1_2/co...        St0
    /testbench/UUT/NUT/\multiple_tg1_2/sig...       St1
    /testbench/UUT/NUT/\multiple_tg1_2/sig...       St1
    /testbench/UUT/NUT/\multiple_tg1_2/sig...       St1
    /testbench/UUT/NUT/\multiple_tg1_2/sig...       St0
    /testbench/UUT/NUT/\multiple_tg1_2/sig...       St0
    /testbench/UUT/NUT/\multiple_tg1_2/en...        St1
    /testbench/UUT/NUT/\multiple_tg1_2/en...        St0
    /testbench/UUT/NUT/\multiple_tg1_2/en...        St0
    /testbench/UUT/NUT/\multiple_tg1_2/en...        St1
  /testbench/UUT/NUT/DONE                           St0
```

Conditional probes

- Conditional probes offer the controlabily that lacks in commercial tools
- Observability can be gained at the cost of adding some variable look-up wires
- … But also using vendor’s tool such as Chipscope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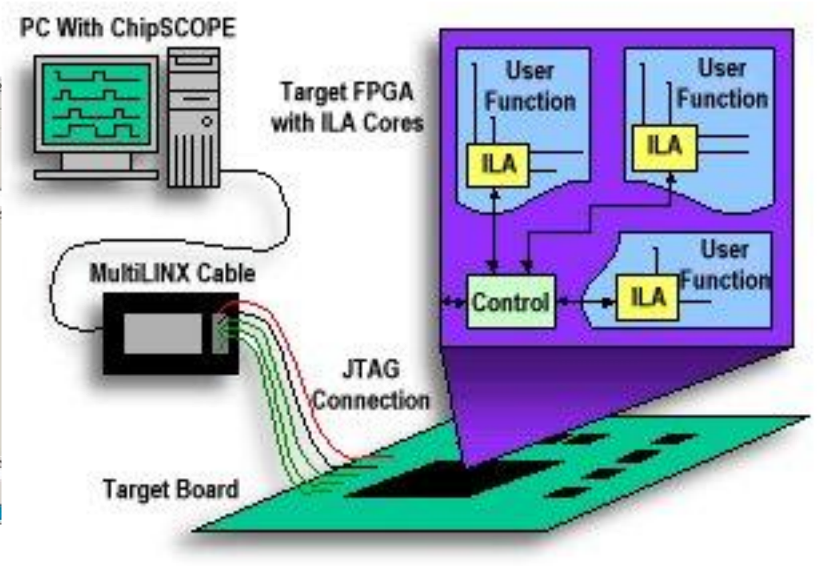
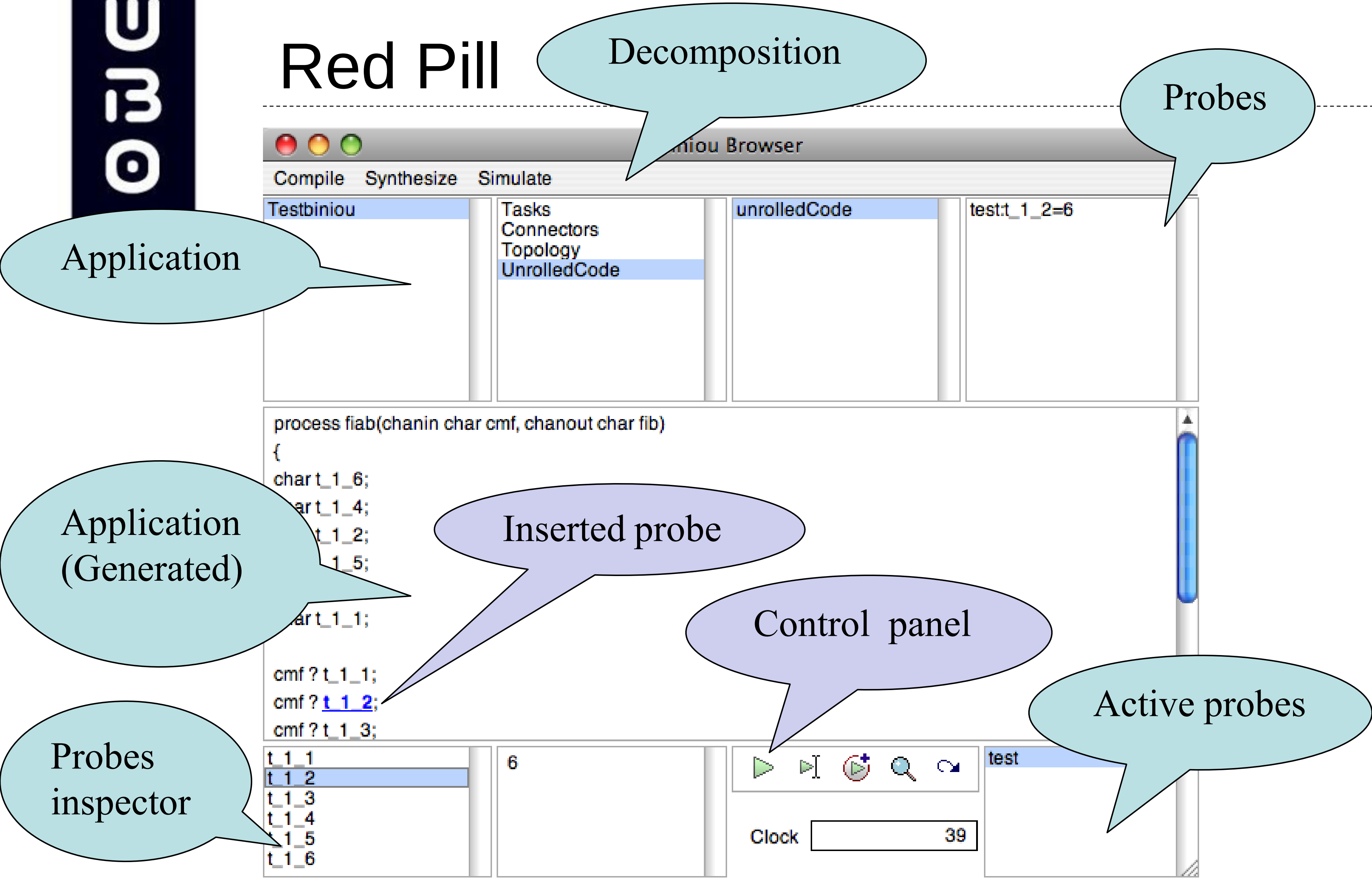
new waveform
Upload
DONE

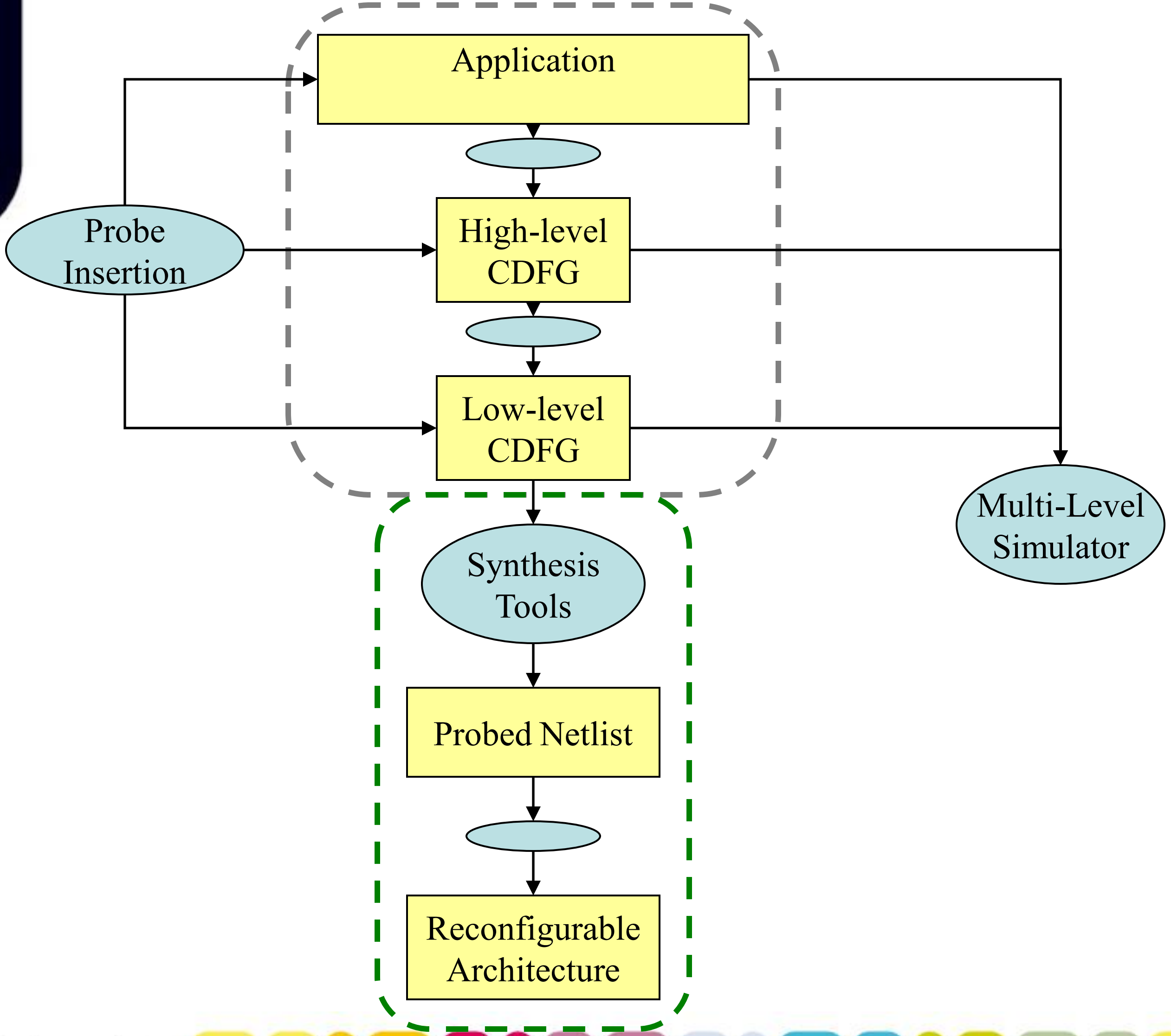


Red Pill



```
process fiab(chanin char cmf, chanout char fib)
{
char t_1_6;
...ar t_1_4;
...t_1_2;
...1_5;

...ar t_1_1;

cmf ? t_1_1;
cmf ? t_1_2;
cmf ? t_1_3;
```

RedPill Flow extends Biniou (HLS)



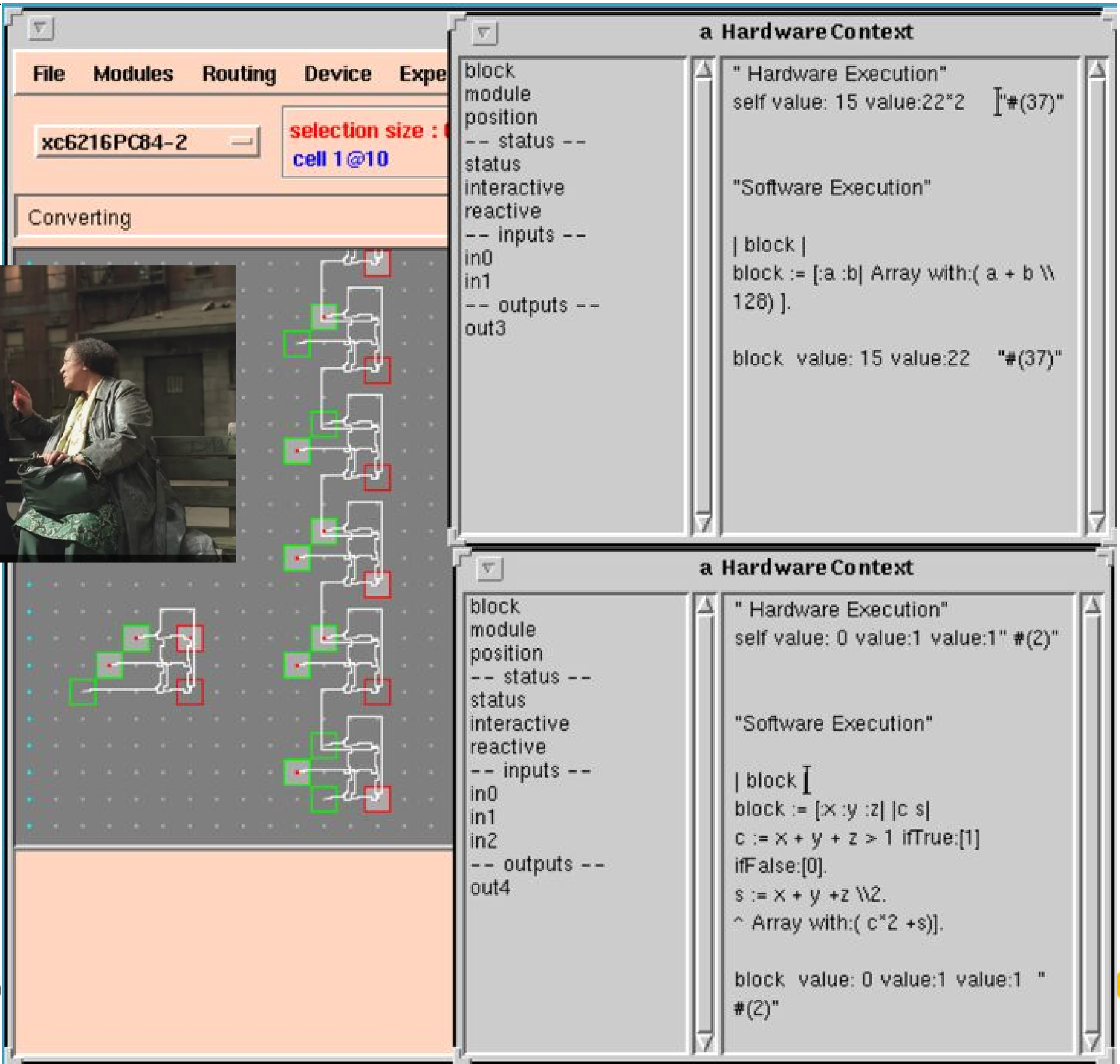
Biniou

Abstract analysis

Encapsulate circuit modules as smalltalk blocks

- Enables soft and hard objects to communicate
- Delivers the power of Sunit to hardware

Abstract analysis (example)



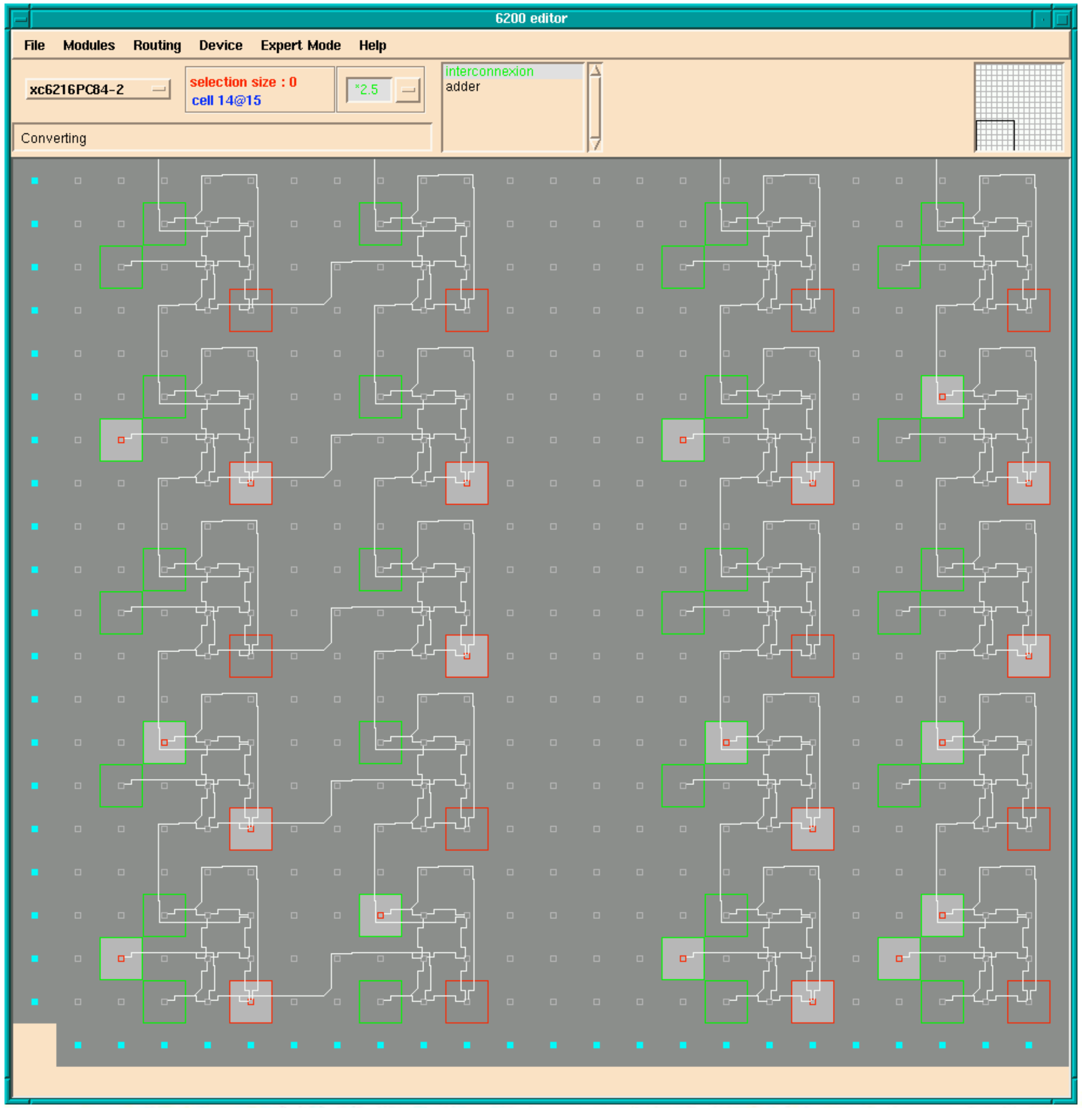
```
block
module
position
-- status --
status
interactive
reactive
-- inputs --
in0
in1
-- outputs --
out3
```

```
" Hardware Execution"
self value: 15 value:22*2    "#(37)"


"Software Execution"

| block |
block := [:a :b| Array with:( a + b \\
128) ].

block  value: 15 value:22    "#(37)"
```

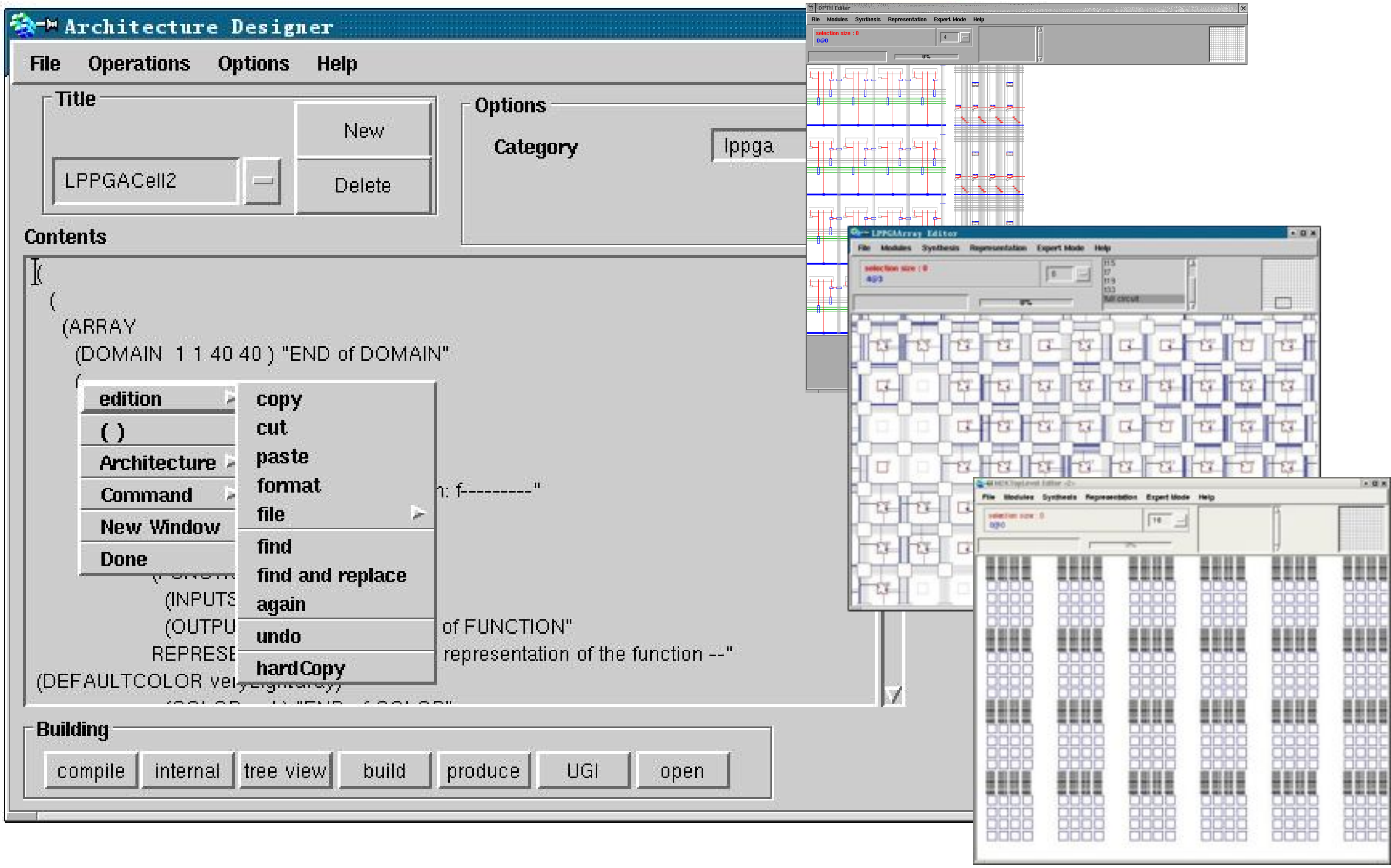
```
block
module
position
-- status --
status
interactive
reactive
-- inputs --
in0
in1
in2
-- outputs --
out4
```

```
" Hardware Execution"
self value: 0 value:1 value:1" #(2)"


"Software Execution"

| block |
block := [:x :y :z| |c s|
c := x + y + z > 1 ifTrue:[1]
ifFalse:[0].
s := x + y +z \\2.
^ Array with:( c*2 +s)].

block  value: 0 value:1 value:1  "
#(2)"
```

Characterization tests & SUnit



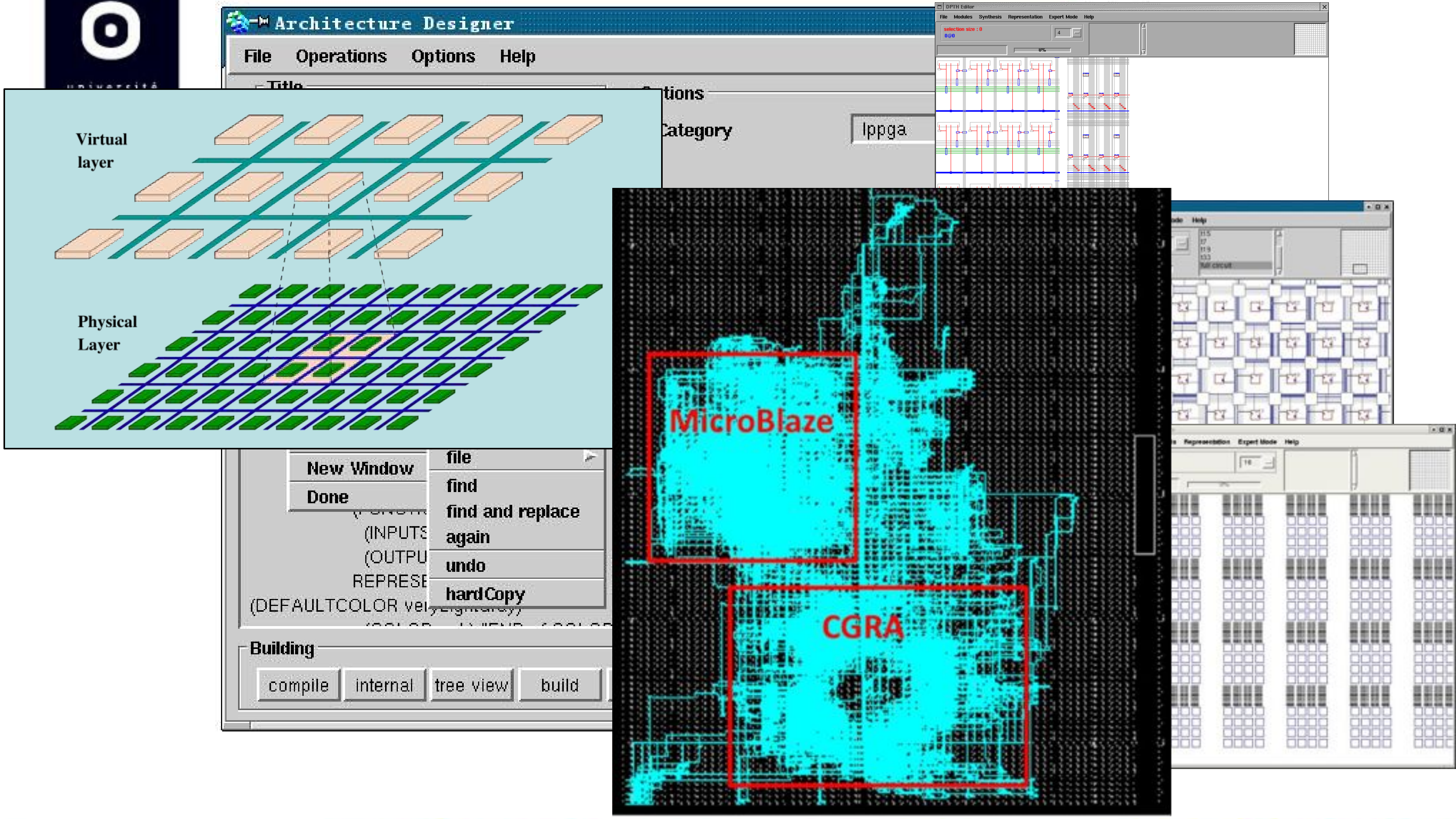
How Many matrix?



Title: LPPGACell2

```
(
 (
  (ARRAY
   (DOMAIN  1 1 40 40 ) "END of DOMAIN"
   (
                                      n: f---------"
         (INPUTS
         (OUTPU                       of FUNCTION"
       REPRESE                        representation of the function --"
(DEFAULTCOLOR ve
```

Reboot the Matrix

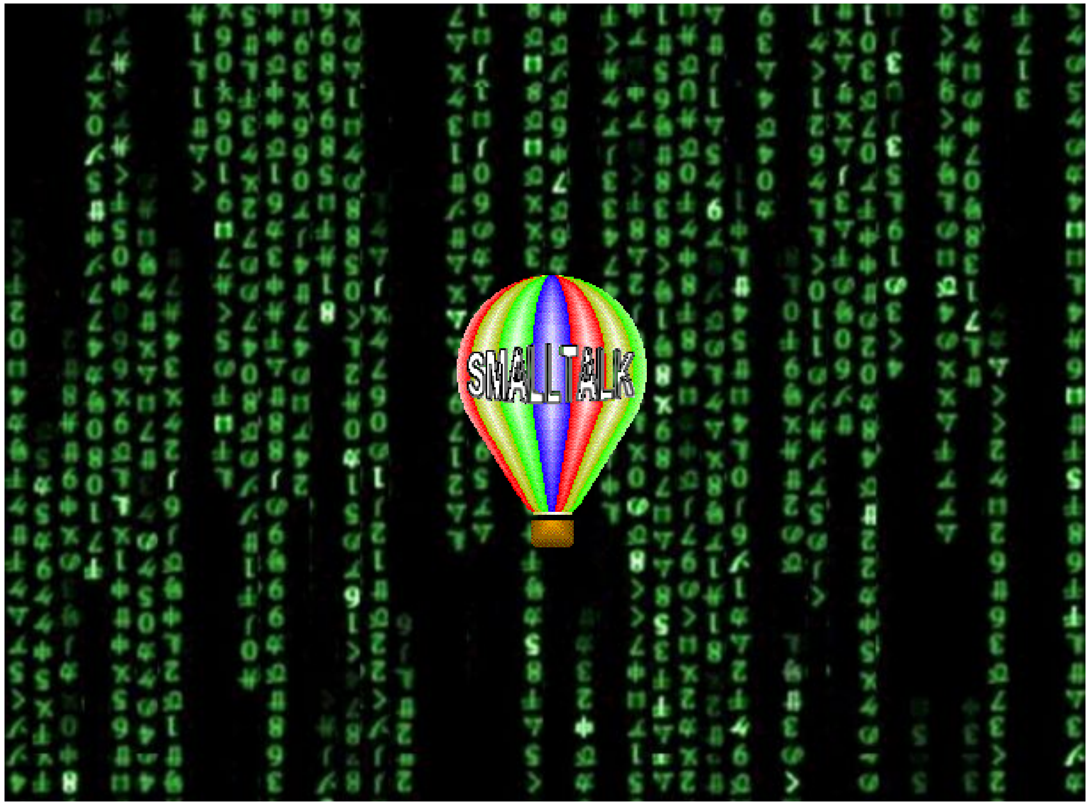


Will you take the red pill?

- HLS (Biniou) offers a path from HL languages to circuits
- Vendors tools offer observability
- Red Pill offers controlability
- Object encapsulation offers abstract analysis and polymorphism.

Smalltalk debug definitively lives in the Matrix

Thank you for your attention



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